IN THE ABSTRACT:

Please insert the Abstract, as follows:

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Abstract Of The Disclosure

An arrangement and a method are provided for replacing defective units, which can be any desired unit of a chip (e.g., arithmetic and logic units), with a function unit. The arrangement and the method provide for performing self-tests more easily, less expensively and before or during a running of an application program. Fault tolerance is greatly enhanced during operation, which is advantageous for failure-critical applications such as in power plants, aviation, space travel or the military, for example.--.

IN THE CLAIMS:

Please cancel original claims 1-17, without prejudice.

Please add the following new claims:

--18. (New) An integrated circuit arrangement, comprising:

at least one module including one of an individual module and a plurality of ordered modules, each module of the at least one module having at least one input and at least one output, the at least one module forming at least one cell, the at least one cell including at least one of a bus system, an arithmetic and logic unit and a configurable logic cell;

a supplementary module assigned to the at least one module and being of a same kind as the at least one module;

a first switching element coupled to the at least one input of a particular module and being upstream from the at least one input of the particular module, the first switching element switching an input signal to at least one of the particular module and a module following the particular module; and

a second switching element coupled to the at least one output of the particular module and being downstream from the at least one output of the particular module,

wherein, if an error occurs in a module, then at least one of a defective

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module and a defective function cell is replaced by a module following the at least one of the defective module and the defective function cell by switching the first switching element and by switching the second switching element, a last module being replaced by the supplementary module.

19. (New) The integrated circuit arrangement according to claim 18, wherein the error is detected via self-testing.

20. (New) The integrated circuit arrangement according to claim 18, further comprising:

a control that controls the first switching element and the second switching element, at least one of (A) the control switching all of the switching elements in the same way and (B) all of the switching elements forming a first group of switching elements and a second group of switching elements, the control switching all of the switching elements in the first group in a first way and switching all of the switching elements in the second group in a second way, the first group and the second group being switched differently to exclude the defective module from the switching elements.

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21. (New) The integrated circuit arrangement according to claim 20, wherein the control is adapted to decode a binary value so as to yield at least one of the first group and the second group.

22. (New) The integrated circuit arrangement according to claim 20, wherein the control is adapted to encode a binary value, the binary value defining at least one of a switching element group and a switching element circuit.

23. (New) The integrated circuit arrangement according to claim 22, wherein the binary value is generated by a counter.

24. (New) The integrated circuit arrangement according to claim 22, wherein the binary value is provided via a look-up-table arrangement.

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25. (New) The integrated circuit arrangement according to claim 18, further comprising:

a memory that stores a binary value, the binary value indicating at least one of the defective module and all defective modules.

26. (New) The integrated circuit arrangement according to claim 25, wherein the memory is independent of a system start.

27. (New) A method for testing an integrated circuit having cells, comprising the steps of:

testing a cell function of the integrated circuit by executing, with the cells, a test program including calculating test vectors;

performing, with at least one of the cells, a comparison between a test result and a setpoint result; and

indicating an error if the comparison indicates a deviation between the setpoint result and the test result so that, in response to the error, a module having the cell found to be defective is replaced.

28. (New) The method according to claim 27, wherein the step of testing the cell function includes the step of testing a cell array by at least one of exchanging and mirroring a test algorithm that includes a plurality of calculations at least once within the cell array.

29. (New) The method according to claim 27, wherein the step of testing the cell function includes the step of calling up test data from an integrated memory in the integrated circuit, the test data being used for executing the test program.

30. (New) The method according to claim 27, wherein the method for testing the integrated circuit is carried out at a system start.

31. (New) The method according to claim 27, wherein the method for testing the integrated circuit is carried out as a self-test method of application programs running during at least one of a wait cycle and an IDLE cycle.

32. (New) The method according to claim 31, wherein the self-test method is at least one of called up from an application program and integrated into an application program.

33. (New) The method according to claim 27, further comprising the steps of:

saving data from arithmetic and logic units to a chip-internal memory before running a test algorithm; and

loading data back into the arithmetic and logic units after running the test algorithm.

34. (New) The method according to claim 33, further comprising the steps of:

shutting down registers in the arithmetic and logic units before running the test algorithm;

using test registers for the test algorithms; and

connecting the registers in the arithmetic and logic units after running the test algorithm.

35. (New) The method according to claim 27, further comprising the steps of:

assigning at least one additional supplementary module to a number of ordered modules forming the cells, the at least one additional supplementary module and the ordered modules being of the same kind, each module having at least one input and at least one output;

coupling a first switching element to the at least one input of a particular module, the first switching element being disposed upstream from the at least one input of the particular module, the first switching element being adapted to switch an input signal to one of the particular module and a module following the particular module;

coupling a second switching element to the at least one output of the particular module, the second switching element being disposed downstream from the at least one output of the particular module, the second switching element being adapted to receive an output from one of the particular module and the module following the particular module; and